AN-9055

Assembly Guidelines for MicroFET 2x2 Dual Packaging

Summary

The Fairchild MicroFET 2x2 dual is a 2mm x 2mm package based on Molded Leadless Packaging (MLP) technology. This technology is often used for power-related products due to its low package height and excellent thermal performance. Large thermal pads in the center of the package solder directly to the Printed Wiring Board (PWB). Modularity in package design, single- and multi-die packages, is within MLP capability.

The MicroFET 2x2 has two large die-attach pads, allowing direct soldering to the PWB for best thermal and electrical performance. The MicroFET 2x2 is designed to be used with Fairchild discrete MOSFET products. This application note focuses on the soldering and back-end processing of the MicroFET 2x2.

Board Mounting

The solder joint and pad design are the most important factors in creating a reliable assembly. The pad dimensions must allow for tolerances in PWB fabrication and pick and place, which are necessary for proper solder fillet formation. MLP packages, when the pre-plated lead-frame is sawn, show bare copper on the end of the exposed edge leads. This is normal and is addressed by IPC JEDEC J-STD-001C "Bottom Only Termination" standard. In practice, optimized PWB pad design and a robust solder process often creates solder fillets to the ends of the lead due to the cleaning action of the flux in the solder paste.

Figure 1. MicroFET 2x2 Dual (Bottom)

PWB Design Considerations

Any land pad pattern must take into account the various PWB and board assembly tolerances for successful soldering of the MLP to the PWB. These factors are considered for the recommended footprint in the datasheet; follow this footprint to assure best assembly yield, thermal performance, and overall system performance.

Figure 2. Exposed Copper on Package Edge, Solder Wetting after Reflow, from Singulation Process

Pad Finish

The MicroFET 2x2 is sold with a lead-free lead finish. Immersion silver, immersion nickel gold, and Organic Surface Protectant (OSP), are the pad finishes of choice for lead-free processing. Hot-air solder-level pad finish does not have chemistry compatibility issues, but is not recommended due to inconsistency in the thickness of the finish. Each finish has useful properties and each has challenges. It is beyond the scope of this paper to debate each system's merits. No one finish is right for all applications, but the most common in large-scale consumer electronics, largely due to cost, is OSP. A high-quality OSP, formulated for the rigors of lead-free reflow, like Enthone® Entek® Plus HT, is recommended.

PWB Material

It is recommended that lead-free FR-4 is used in PWB construction. Lower-quality FR-4 can cause numerous problems with the reflow temperatures seen when using lead-free solder. IPC-4101B "Specification for Base Materials for Rigid and Multilayer Printed Boards" contains further information on choosing the correct PWB material for the intended application.

Using Vias with MicroFET 2x2

Designers often wish to place vias inside the thermal pads. While this is understandable, the vias often create voiding and appropriately sized vias for the small pads can be quite costly in production. Previous studies have shown the vias can be placed just outside the pad and excellent performance still achieved.

Stencil Design

It is estimated that 60% of all assembly errors are due to paste printing. For a controlled, high-yielding manufacturing process; it is, therefore, the most critical phase of assembly. Due to the importance of the stencil design, many stencil types have been characterized to determine the optimal stencil design for the datasheet recommended footprint pad on a typical application board with OSP surface finish on FR-4. The paste was printed from a laser-cut 4-mils thick stainless steel stencil. Two stencil recommendations are given in the appendix. The best performance was found with the split solder print on the drain tab. However, both solder apertures were proven to work well. The paste was printed on the outer pins with a slightly reduced ratio to the PWB pad. IPC-7525 "Stencil Design Guidelines" gives a formula for calculating the area ratio for paste release prediction:

$$Area\ Ratio = \frac{Area\ of\ \ Pad}{Area\ of\ \ Aperture\ Walls} = \frac{L * W}{2 * (L * W) * T} \quad (1)$$

where L is the length, W the width, and T the thickness of the stencil. When using this equation, an area ratio >0.66 should yield acceptable paste release.

For MicroFET 2x2 dual, it is recommended that the solder screen be opened to cover 60% of the inner and outer pads when using a 4-mils (0.10mm) thick stencil. A drawing is the appendix. A modified inverse homeplate design was chosen to optimize beading and voiding for production.

Solder Paste

The MicroFET 2x2 is a RoHS-compliant and lead-free package. The lead finish is NiPdAu. Any standard lead-free no clean solder paste commonly used in the industry should work with this package. The IPC Solder Products Value Council has stated that the lead-free alloy, 96.5Sn/3.0Au/0.5Cu, commonly known as SAC 305, is "…the lead-free solder paste alloy of choice for the electronics industry." Type-3 no-clean paste, SAC 305 alloy, was used for the construction of the boards studied to optimize the process.

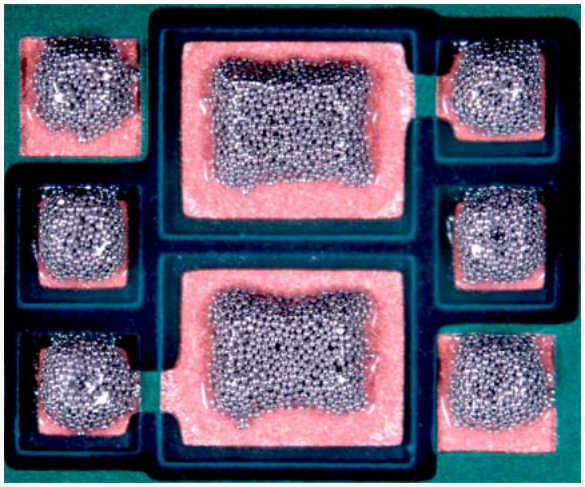


Figure 3. Printed Solder Paste, Recommended Print

Reflow Profile

The optimum reflow profile used for every product and oven is different. Even the same brand and model oven in a different facility may require a different profile. The proper ramp and soak rates are determined by the solder paste vendor for their specific products.

Obtaining this information from the paste vendor is highly recommended. If using a KIC® profiler, download the latest paste library from KIC yield ramp rate and soak times at temperatures for most commonly used solder pastes. Using this data, the software optimizes the zone set-points and conveyor speed. The Fairchild MicroFET 2x2 is rated for 260ºC peak temperature reflow. The appendix contains a sample reflow profile used for building demonstration boards. This profile is provided for reference only; different PWBs, ovens, and pastes changes this profile, perhaps dramatically.

Voiding

Voiding is a very controversial topic in the industry. The move to lead-free solders has driven the need for intense study in the area of solders, solder joints, and reliability effects. There are varying viewpoints on the effect of vias and allowable quantity. There are several types of voids; for simplicity this applications note classifies them into two categories, macro voids and micro voids.

Macro voids could also be called process voids. Macro voids are the large-sized voids commonly seen on x-ray during inspection. These voids are due to process design, process control issues, or PWB design issues. All of the parameters discussed in this application note effect macro-voiding. Most standards that currently exist, such as IPC-610D, specifically address void criteria for BGA and limit it to 25%. This standard is for macro voiding.

There is currently no industry standard for macro voiding in MLP solder joints. Fairchild has completed several reliability studies, characterizing voiding in various types of components with large thermal pads and the effect on reliability. It was found that components with ≤25% voiding exhibit acceptable reliability performance in package qualification temperature cycling. Fairchild suggests the 25% as maximum voiding for MLP type packages.

There are also several forms of micro-voiding, planar micro voids and Kirkendall voids. The mechanism of void creation is different for each and both are practically undetectable by x-ray inspection. Both types are also currently the subject of several in-depth studies; however, none have confirmed theories of creation.

Planar micro voids, or “champagne voids,” occur at the PWB land-to-solder-joint interface. There are several theories on the mechanism that creates planar micro voids, but there is no industry consensus on the causal mechanism. Planar micro voids are a risk for reliability failures.

Kirkendall voids are created at the interface of two dissimilar metals at higher temperatures; in the case of solder attachments, at the pad to joint intermetallic layer. They are not due to the reflow process; Kirkendall voids are created by electromigration in assemblies that spend large amounts of time above 100ºC. There is conflicting evidence on whether or not Kirkendall voids are a reliability risk.

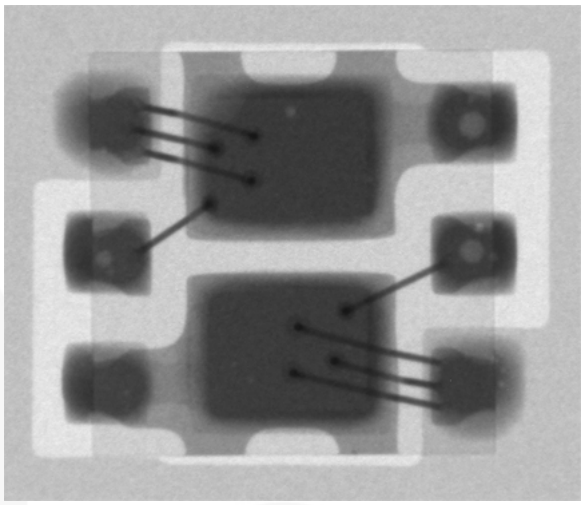


Figure 4. X-Ray Image Showing Voiding Caused by Normal Process Variation during Reflow

Rework

Due to the high temperatures associated with lead-free reflow, it is recommended that this component not be reused if rework becomes necessary. The MicroFET 2x2 should be removed from the PWB with hot air. After removal, the MicroFET 2x2 should be discarded. The solder remnants should be removed from the pad with a solder vacuum or solder wick, the pads cleaned, and new paste printed with a mini stencil. Localized hot air can be applied to reflow the solder and make the joint. Due to the thermal performance of this component and the high performance PWB it is mounted on, quite a bit of heat energy is necessary. Heating of the PWB may be helpful for the rework process.

Board-Level Reliability

Per JDC-STD-001D, a solder fillet is not required on the side of the lead for this package; but it has been found through modeling and temperature cycling that a solder fillet on the lead end can improve reliability. An improvement of 20% can be expected with this fillet. It has also been found that the 20% reliability enhancement is attained even when the fillet only wets halfway up the side of the lead. Expect to create reliability enhancing solder fillets through proper process design and control.

As part of the standard reliability testing, this package was temperature cycled from -10°C to 100°C. There should be no failures in the sample set at 1000 cycles to pass the test.

Appendix

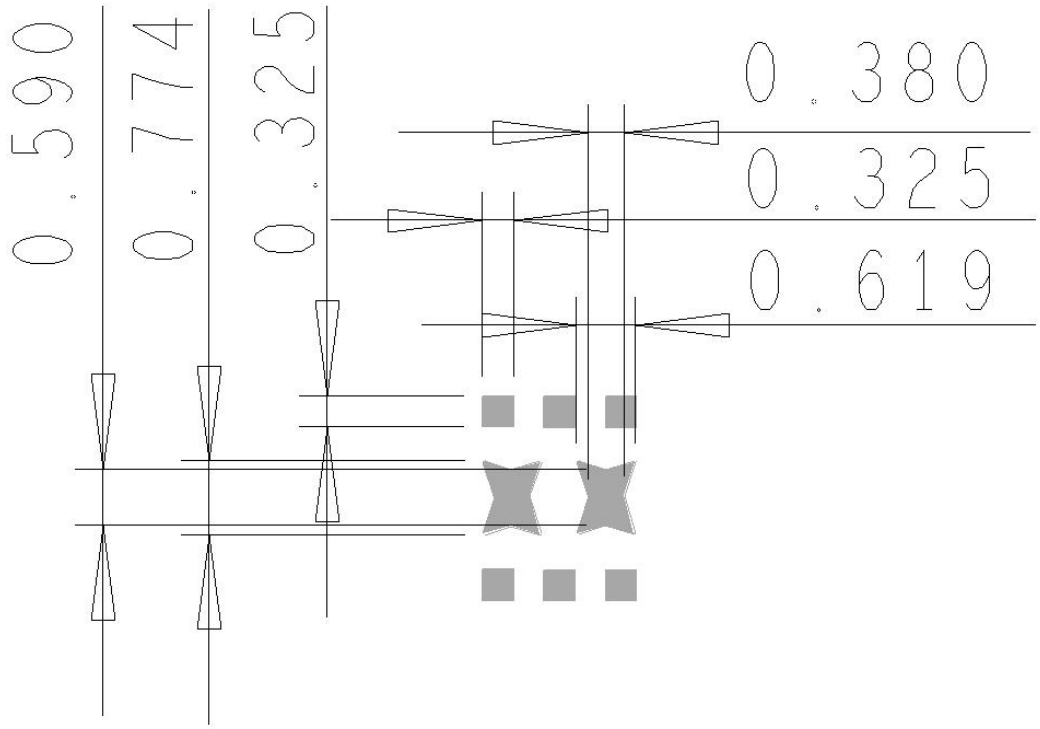
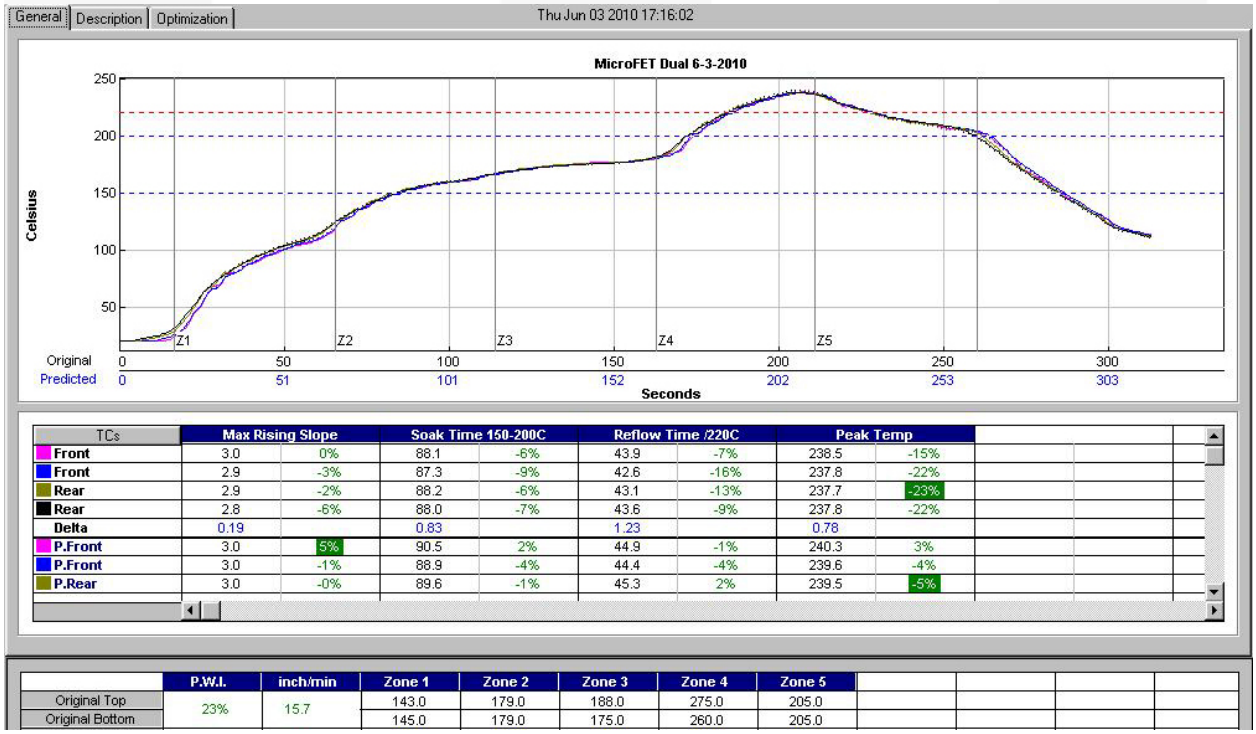


Figure 5. Solder Stencil Opening Recommendations (mm)



TCs	Max Rising Slope		Soak Time 150-200C		Reflow Time /220C		Peak Temp	
Front	3.0	0%	88.1	-6%	43.9	-7%	238.5	-15%
Front	2.9	-3%	87.3	-9%	42.6	-16%	237.8	-22%
Rear	2.9	-2%	88.2	-6%	43.1	-13%	237.7	-23%
Rear	2.8	-6%	88.0	-7%	43.6	-9%	237.8	-22%
Delta	0.19		0.83		1.23		0.78	
P.Front	3.0	5%	90.5	2%	44.9	-1%	240.3	3%
P.Front	3.0	-1%	88.9	-4%	44.4	-4%	239.6	-4%
P.Rear	3.0	-0%	89.6	-1%	45.3	2%	239.5	-5%

	P.W.I.	inch/min	Zone 1	Zone 2	Zone 3	Zone 4	Zone 5
Original Top	23%	15.7	143.0	179.0	188.0	275.0	205.0
Original Bottom			145.0	179.0	175.0	260.0	205.0

Figure 6. Reflow Profile used for Building Demonstration Boards

Related Resources

[1] Aspandiar, Raiyo, "Voids in Solder Joints," SMTA Northwest Chapter Meeting, September 21, 2005, Intel® Corporation.

[2] Bryant, Keith, "Investigating Voids," Circuits Assembly, June 2004.

[3] Comley, David, et al, "The QFN: Smaller, Faster and Less Expensive," Chip ScaleReview.com, August/September 2002.

[4] Englemaier, Werner, "Voids in Solder Joints-Reliability," Global SMT & Package, December 2005.

[5] IPC Solder Products Value Council, "Round Robin Testing and Analysis of Lead Free Solder Pastes with Alloys of Tin, Silver and Copper," 2005.

[6] IPC-A-610-D, "Acceptance of Electronic Assemblies," February 2005.

[7] IPC J-STD-001D, "Requirements for Soldered Electrical and Electronic Assemblies."

[8] IPC-SM-7525A, "Stencil Design Guidelines," May 2000.

[9] JEDEC, JESD22-B102D, "Solderability," VA, Sept. 2004.

[10] Syed, Ahmer, et al, "Board-Level Assembly and Reliability Considerations for QFN Type Packages," Amkor Technology, Inc., Chandler, AZ.